



Once it completes the 15-button sequence (LastIndex is 14 and Done is 1), the user has won, and the module will be reset via its Reset input.

Hasbro will allow you to modify the behavior of its product at the start of a game, if that turns out to be convenient, as long as the initial behavior is reasonable. Examples of reasonable behavior include skipping over the initial one-button sequence and/or displaying no lights for a clock cycle previous to displaying the first sequence. The Done output, though, must be 1 only once the module has displayed the full initial sequence; and the LastIndex output must always be one less than the length of the current sequence.

I will locate and place some Web links concerning Verilog onto the Assignments page. Additionally, the textbook includes quite a bit of information in Appendix B and Section 5.8, which are packaged on the CD — and the CD also incorporates a very thorough tutorial about Verilog. Note that opening the CD package in the book will likely reduce its resale value markedly; I will be happy to loan my CD to anybody who can demonstrate ownership of the textbook, to permit copying the CD contents without dramatically reducing the resale value. (Of course, you'd need to delete the copy should you choose to resell the book.)

To compile your work, execute the following:

```
unix% iverilog -o Driver.vvp Driver.v
```

And to simulate it:

```
unix% vvp Driver.vvp | more
```

Verilog is nice for designing circuits, because it removes you from worrying about individual gates. Unfortunately, this leads to a real pitfall: That you inadvertently create a more complex circuit than is needed. Particularly problematic is adding state-based computation where the computation really ought to be combinational. To avoid state, do the following whenever possible:

- Prefer placing information in `assign` blocks (which are always combinational) rather than `always` blocks.
- Each input signal used in an `always` block should appear in its `@` list.
- If you assign to a `reg` on any path in an `always` block, make sure the same `reg` is assigned on *all* paths. Of course, it may be assigned to keep its old value.
- The above means that every `if` will have an `else`, and every `case` will have a `default`.